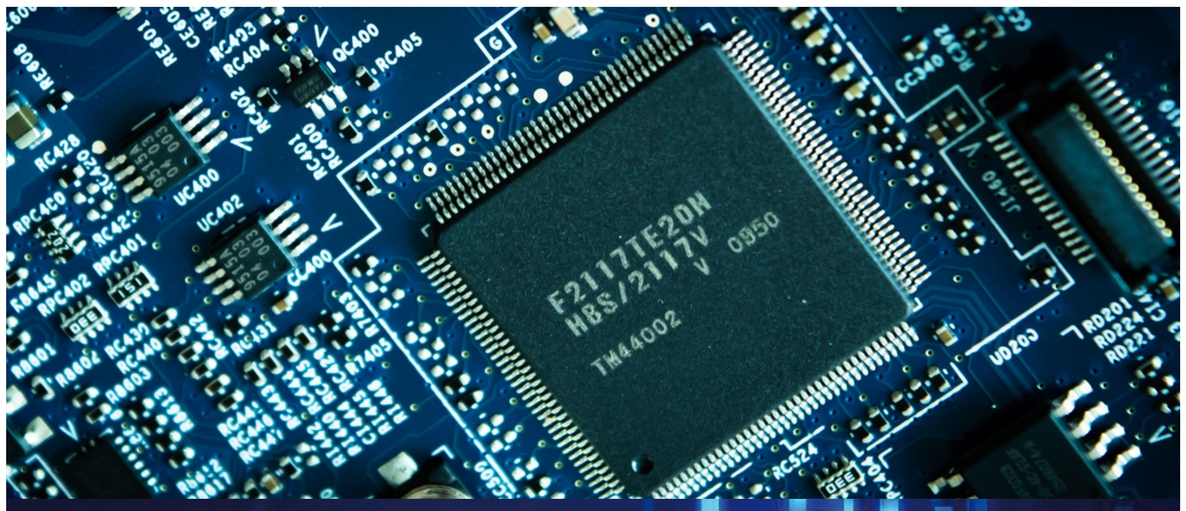
eProcessor



Open Source RISC-V Full Hardware and Software stack

eProcessor.eu @eprocessor_eu eProcessor

OBJECTIVES

- The **eProcessor project** aims to build a new open source Out of Order (OoO) processor and deliver the first open source European full-stack ecosystem based on this new RISC-V CPU.
- **eProcessor technology** will be extendable (open source), energy efficient (low power), extreme-scale (high performance), suitable for uses in HPC and embedded applications, and extensible (easy to add on-chip and/or off-chip components).
- The project is **an ambitious combination** of processor design, based on the RISC-V open source hardware ISA, applications and system software extending pre-existing Intellectual Property (IP), combined with new IP that can be used as building blocks for future HPC systems, both for traditional and emerging application domains.

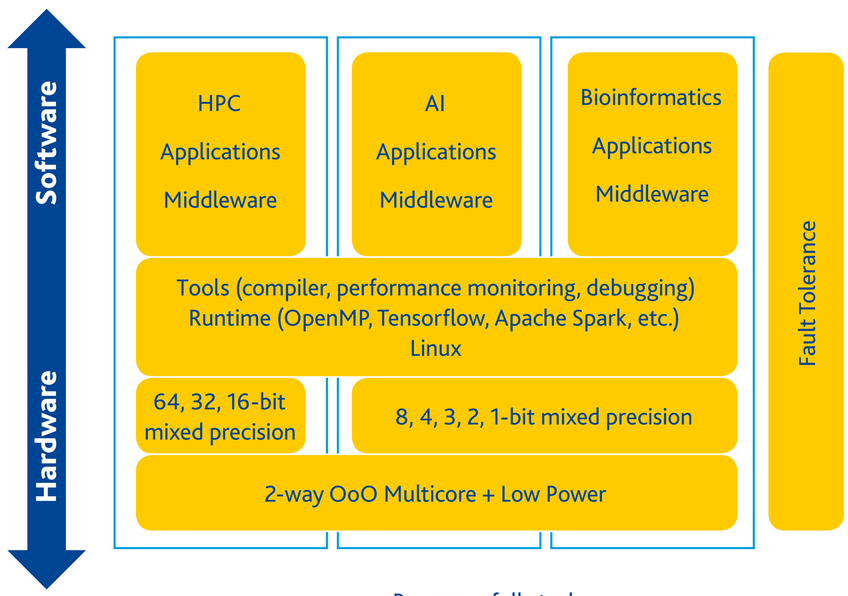
Thus eProcessor aims at :

1. Expanding European capabilities around the development of an actual IC chip.
2. Improving and extending the open system software stack for RISC-V, providing new software to run on this novel hardware.
3. Demonstrate, validate and benchmark using applications from the area of Smarthome and Surveillance.

AMBITION

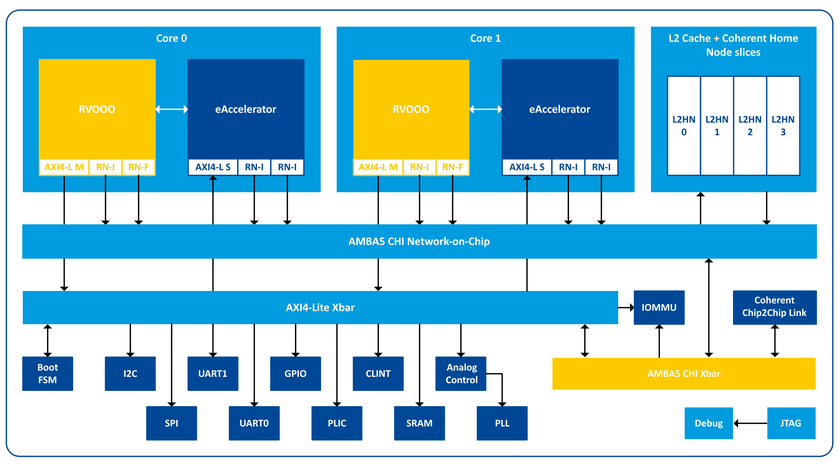
- eProcessor goes beyond the traditional **HPC** usage domain, expands to **High Performance Data Analytics (HPDA) and Deep Learning and AI workloads**, and mixed-precision processing technologies for genomic processing in the Bioinformatics domain.
- Explore new areas in reduced precision, sparsity, and software/hardware co-design.
- Allow the OpenMP runtime and compiler to guide cache coherence optimizations and to implement energy-efficient scheduling and synchronization; as well as to integrate Tensorflow and Apache Spark ML.
- Advance the state-of-the-art for the ML accelerators by developing arithmetic units to support simultaneously a wide range of **reduced and mixed precision** (1, 2, 4, 8-bit) as well as explore new formats (8- and 16-bit bfloat) for reduced precision floating-point for ML training;
- Improve application performance using cooperative **adaptive on-chip memories** (scratchpad for last-level cache)
- Devise a **Coherent CPU/Accelerator Interconnect and NoC**;
- Provide **Fault Tolerance** for critical processor structures such as L1 Data & Instruction caches, L2 cache, TLB, and register files with various error detection strengths (parity or lightweight ECC).

APPROACH



eProcessor full stack

- Software/hardware co-design for improved application performance & system energy efficiency
  - HPC
  - HPDA (AI/ML/DL)
  - Bioinformatics
- Europe's first Open Source high performance Out-of-Order (OoO) 64-bit RISC-V platform
  - 2-way OoO Core
  - Single core & multi-core: 2 tapeouts
  - Multi-socket, cache coherent implementation
  - Adaptive caches
- On chip Vector + AI accelerator
  - New Bioinformatics accelerator co-processor
- Coherent off-chip accelerator: CNN



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extoll latency matters.
EXAPSYS

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